



Product Specification

AU OPTRONICS CORPORATION

(V) Preliminary Specifications

() Final Specifications

Module	13.3"(13.25") HD 16:9 Color TFT-LCD Open Cell
Model Name	B133XW04 V2 (H/W: 0A)

Customer

Date

Checked &
Approved by

Date

Note: This Specification is subject to change without notice.

Approved by

Date

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Prepared by

Kay CY Wang10/29/2010

NBBU Marketing Division
AU Optronics corporation



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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2010/10/29	All	First Edition for Customer		



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1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the product.
- 8) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT LCD.
- 9) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentarily. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 10) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 11) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.



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2. General Description

B133XW01 V4 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD, 1366(H) x 768(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

B133XW01 V4 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	13.3W”(13.25)			
Active Area	[mm]	293.42 x 164.97			
Pixels H x V		1366 x 3(RGB) x 768			
Pixel Pitch	[mm]	0.2148 x 0.2148			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
Response Time	[ms]	8 typ / 16 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Weight	[Grams]	175 max.			
Physical Size	[mm]		Min.	Typ.	Max.
		Length	---	---	302.927
		Width	---	---	216.866
		Thickness	---	---	1.4
Electrical Interface		1 channel LVDS			
Glass Thickness	[mm]	0.5			
Surface Treatment		Glare, Hardness 3H			
Support Color		262K colors (RGB 6-bit)			
RoHS Compliance		RoHS Compliance			

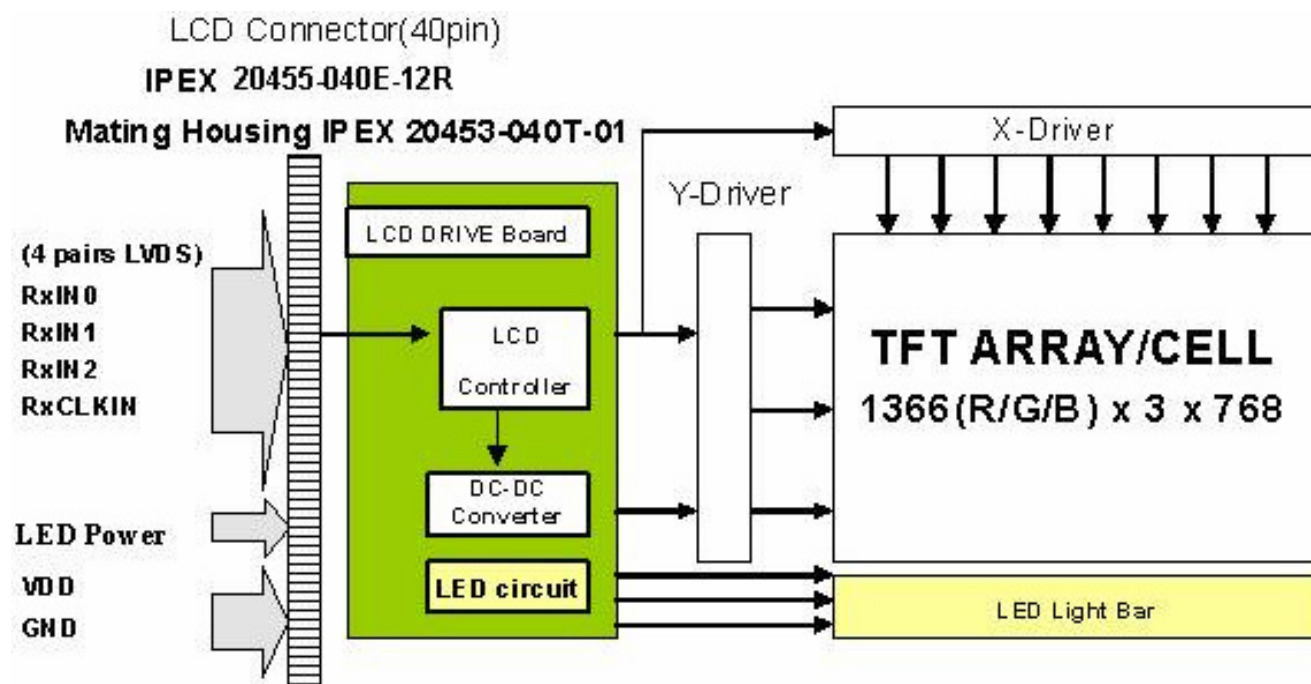


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3. Functional Block Diagram

The following diagram shows the functional block of the 13.3 inches wide Color TFT/LCD 40 Pin one channel Module





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4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values



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5. Electrical Characteristics

5.1 TFT LCD

5.1.1 Power Specification

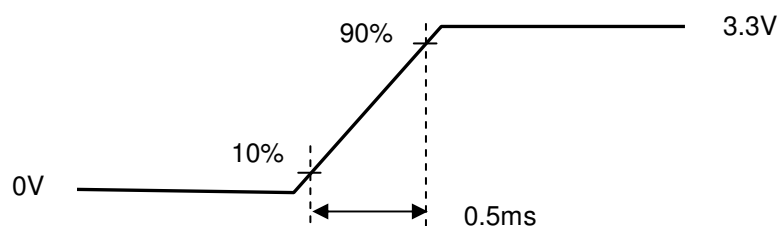
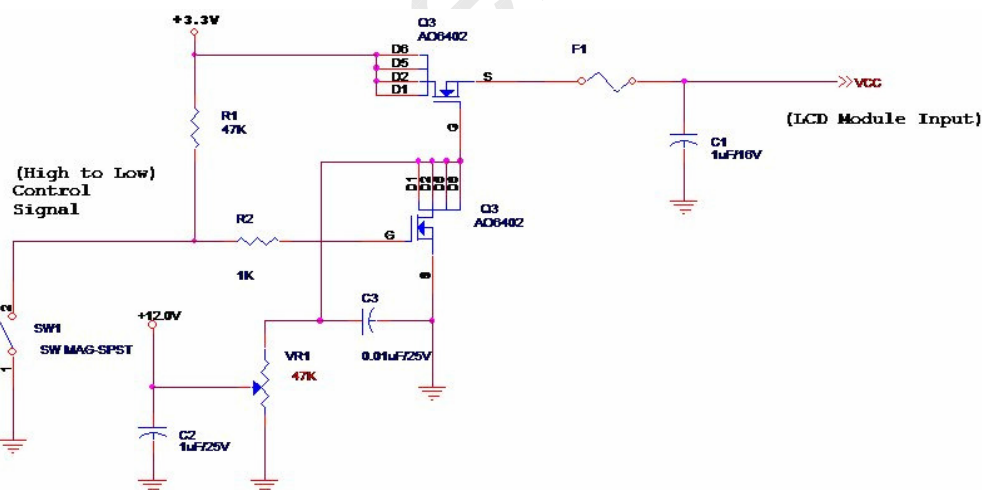
Input power specifications are as follows;

The power specification are measured under 25°C and frame frequency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1.0	[Watt]	Note 1
IDD	IDD Current	-	-	300	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern at 3.3V driving voltage. ($P_{\max} = V_{3.3} \times I_{\text{black}}$)

Note 2 : Measure Condition



Vin rising time



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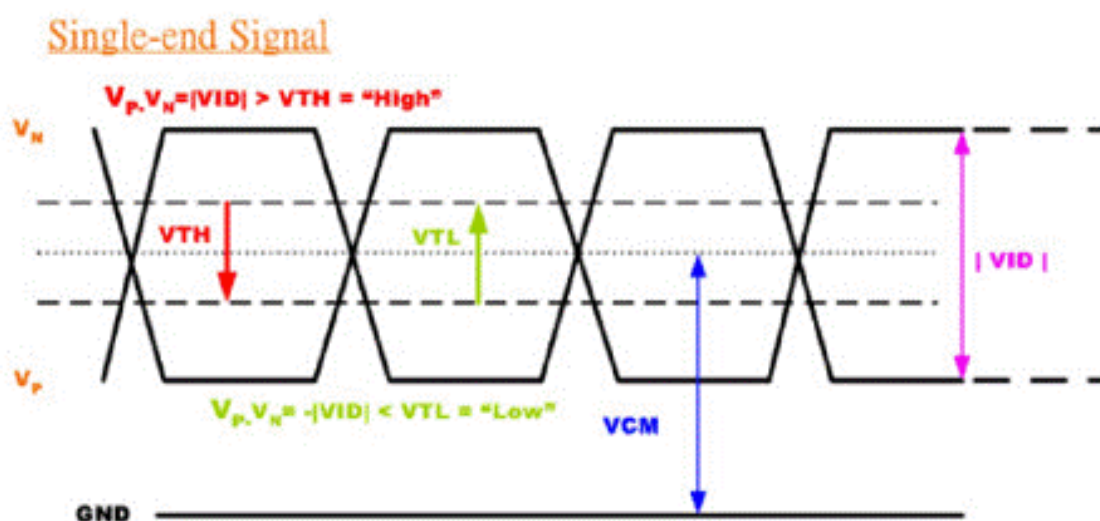
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
V_{TH}	Differential Input High Threshold ($V_{cm}=+1.2V$)	---	100	[mV]
V_{TL}	Differential Input Low Threshold ($V_{cm}=+1.2V$)	-100	---	[mV]
$ V_{ID} $	Differential Input Voltage	100	600	[mV]
V_{CM}	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Wavefor



6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.

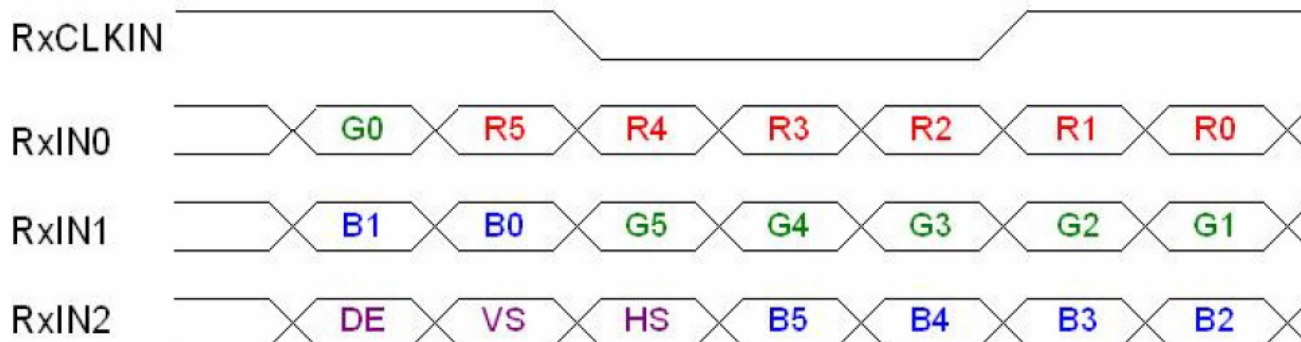
	1			2												1365			1366		
1st Line	R	G	B	R	G	B	-									R	G	B	R	G	B
	.	.	.	.	.	.	.									.	.	.	.	.	.
	.	.	.	.	.	.	.									.	.	.	.	.	.
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	.	.	.	.	.	.	.									.	.	.	.	.	.
	.	.	.	.	.	.	.									.	.	.	.	.	.
768th Line	R	G	B	R	G	B	-									R	G	B	R	G	B



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6.2 The Input Data Format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB)	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
	Red-pixel Data	
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB)	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
	Green-pixel Data	
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB)	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
	Blue-pixel Data	
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.



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6.3 Integration Interface Requirement

6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or Compatible
Type / Part Number	IPEX 20455-040E-12R or Compatible
Mating Housing/Part Number	IPEX 20453-040T-01 or Compatible

6.3.2 Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

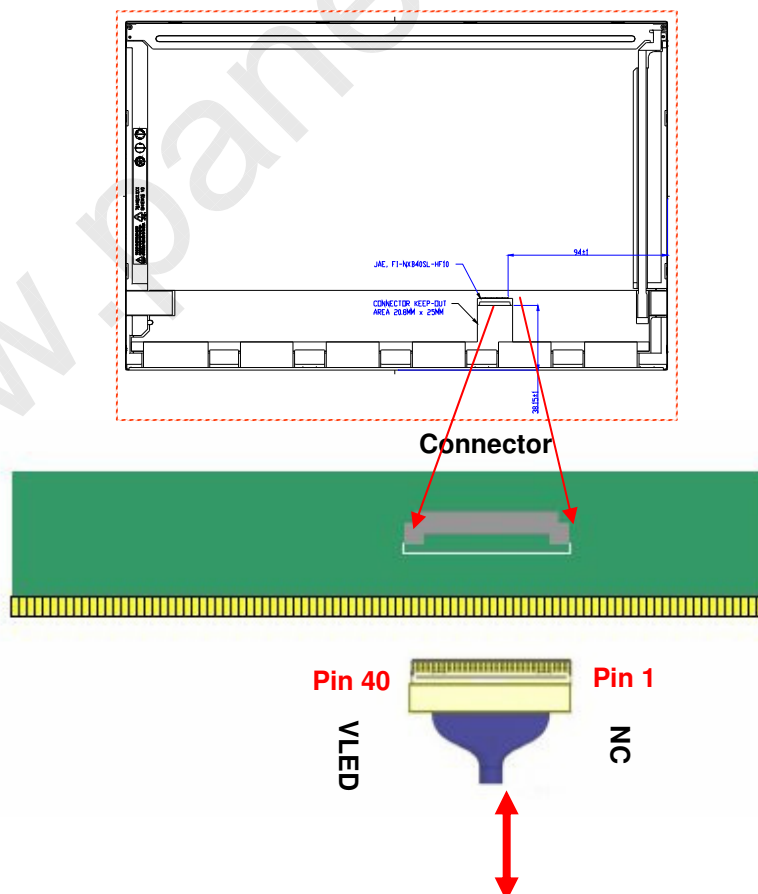
PIN#	Signal Name	Description
1	NC	No Connection (Reserve)
2	VDD	Power Supply +3.3V
3	VDD	Power Supply +3.3V
4	VEDID	EDID +3.3V Power
5	NC	No Connect (Reserve)
6	CLK_EDID	EDID Clock Input
7	DAT_EDID	EDID Data Input
8	RxOIN0-	-LVDS Differential Data INPUT(Odd R0-R5,G0)
9	RxOIN0+	+LVDS Differential Data INPUT(Odd R0-R5,G0)
10	VSS	Ground
11	RxOIN1-	-LVDS Differential Data INPUT(Odd G1-G5,B0-B1)
12	RxOIN1+	+LVDS Differential Data INPUT(Odd G1-G5,B0-B1)
13	VSS	Ground
14	RxOIN2-	-LVDS Differential Data INPUT(Odd B2-B5,HS,VS,DE)
15	RxOIN2+	+LVDS Differential Data INPUT(Odd B2-B5,HS,VS,DE)
16	VSS	Ground
17	RxOCKIN-	-LVDS Odd Differential Clock INPUT
18	RxOCKIN+	-LVDS Odd Differential Clock INPUT
19	IMG_EN	Color Management Input Level
20	NC	No connection
21	NC	No connection
22	NC	No connection



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23	NC	No connection
24	NC	No connection
25	NC	No connection
26	NC	No connection
27	NC	No connection
28	NC	No connection
29	NC	No connection
30	NC	No connection
31	VLED_GND	LED Ground
32	VLED_GND	LED Ground
33	VLED_GND	LED Ground
34	NC	No Connection (Reserve)
35	VPWM_EN	PWM logic input level
36	VLED_EN	LED enable input level
37	DCR_EN	Dynamic Contrast Ratio Input Level
38	VLED	LED Power Supply 6V-21V
39	VLED	LED Power Supply 6V-21V
40	VLED	LED Power Supply 6V-21V



Note1: Input signals shall be low or High-impedance state when VDD is off.



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Note1: Input signals shall be low or High-impedance state when VDD is off.

6.4 Interface Timing

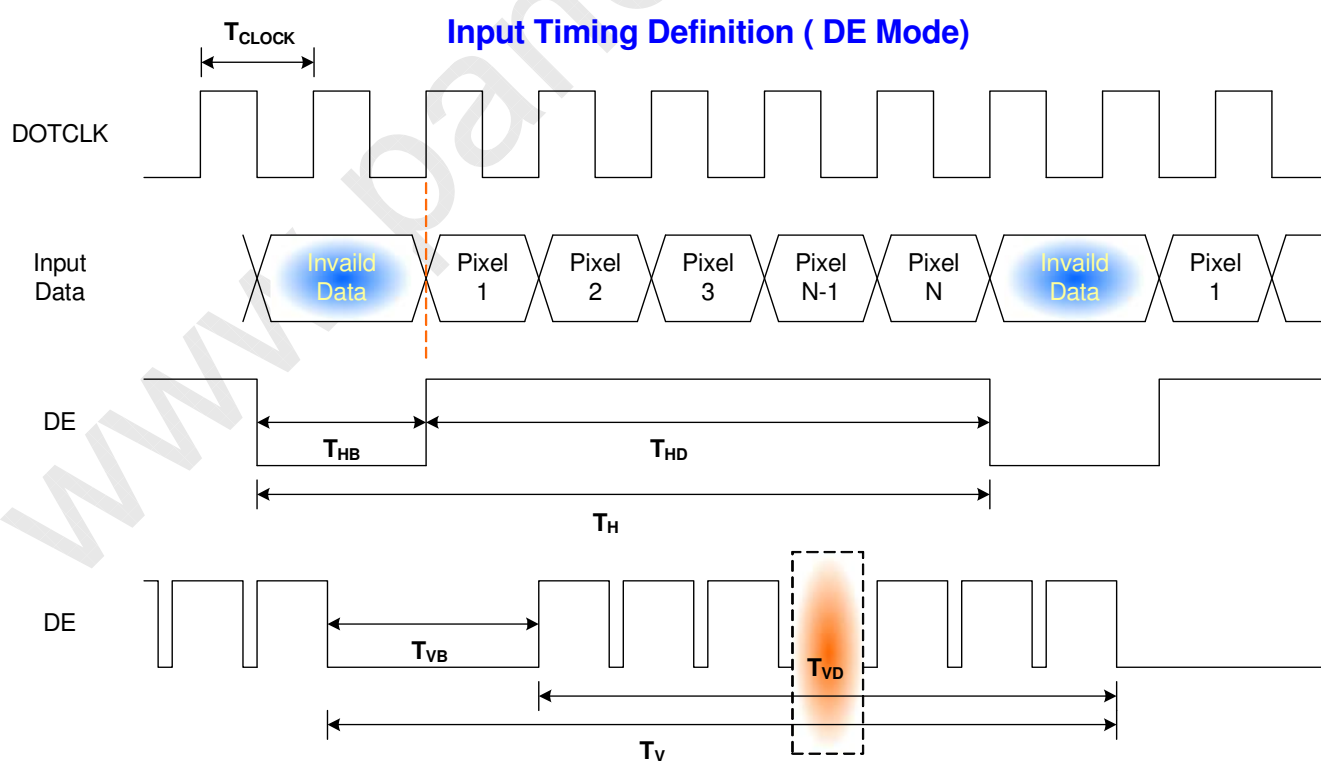
6.4.1 Timing Characteristics

Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	---	60	---	Hz
Clock frequency		1/ T _{Clock}	65	69.3	80	MHz
Vertical Section	Period	T _V	776	793	1000	T _{Line}
	Active	T _{VD}	768			
	Blanking	T _{VB}	8	25	232	
Horizontal Section	Period	T _H	1426	1456	2000	T _{Clock}
	Active	T _{HD}	1366			
	Blanking	T _{HB}	60	90	634	

Note : DE mode only

6.4.2 Timing diagram



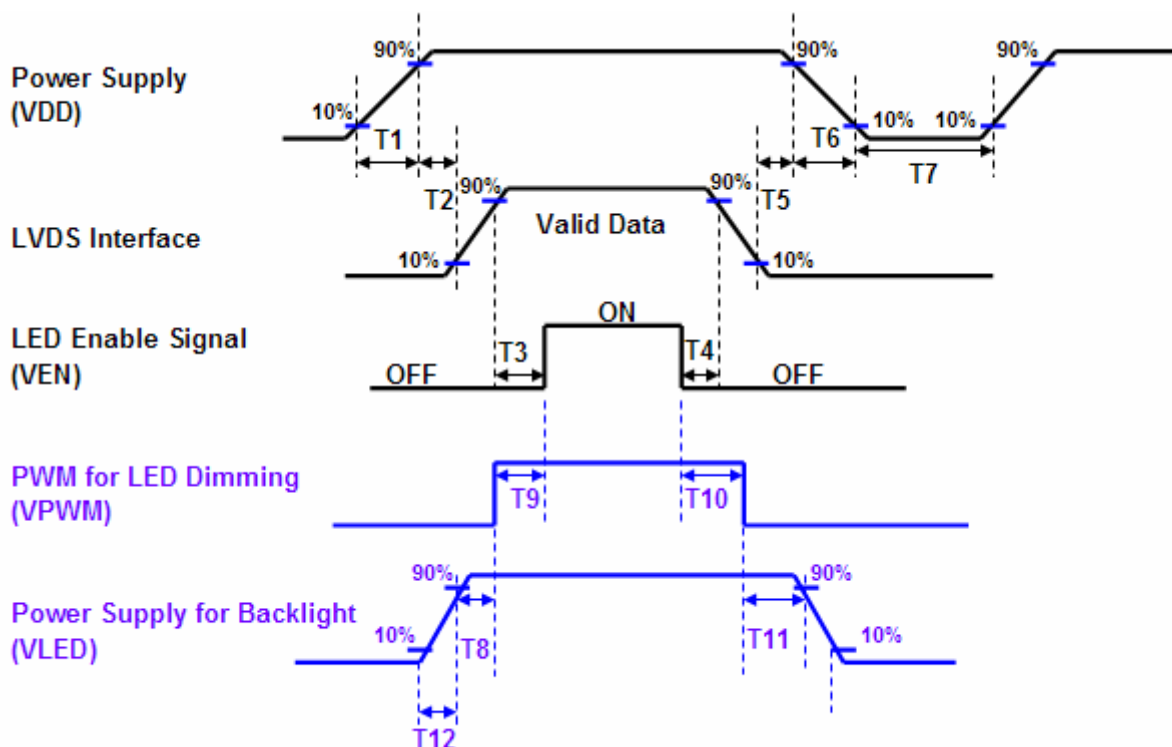


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6.5 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Power Sequence Timing			
Parameter	Value		Units
	Min.	Max.	
T1	0.5	10	ms
T2	0	50	
T3	200	-	
T4	200	-	
T5	0	50	
T6	0	10	
T7	500	-	
T8	10	-	
T9	10	180	
T10	10	180	
T11	10	-	
T12	0.5	10	



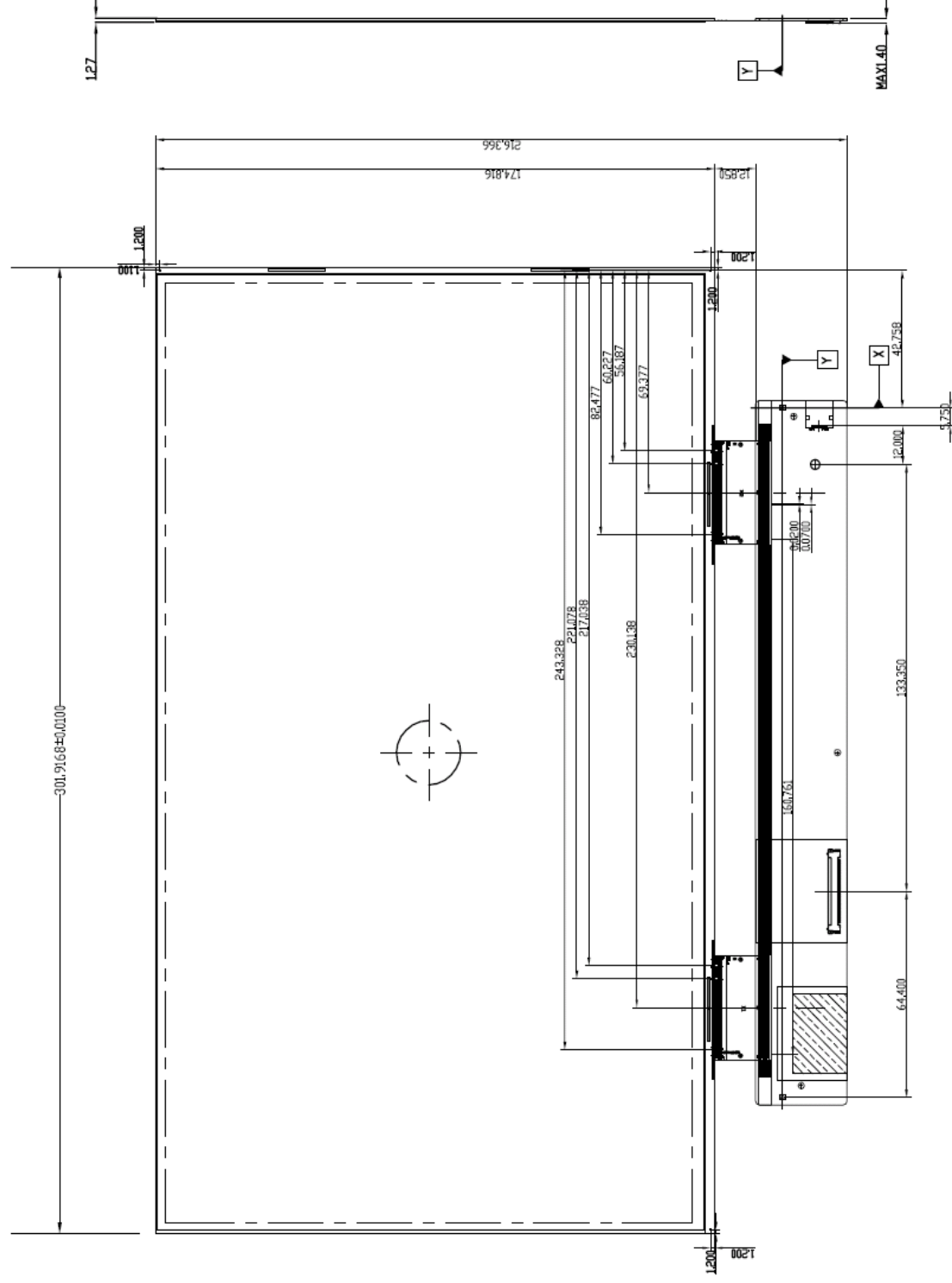
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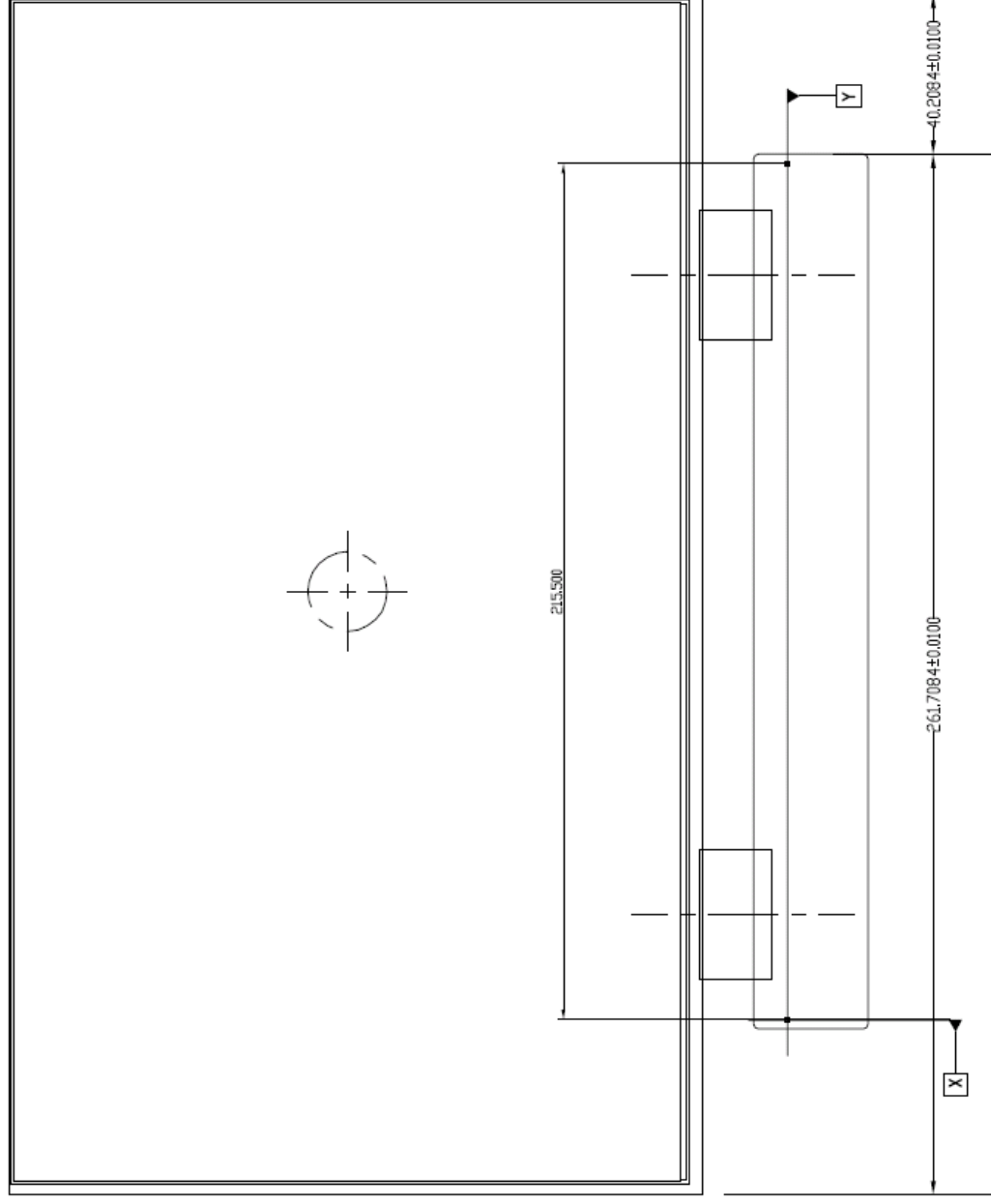
7. Mechanical Characteristics

7.1 LCD Outline Dimension

7.1.1 Standard Front View



7.1.2 Standard Rear View

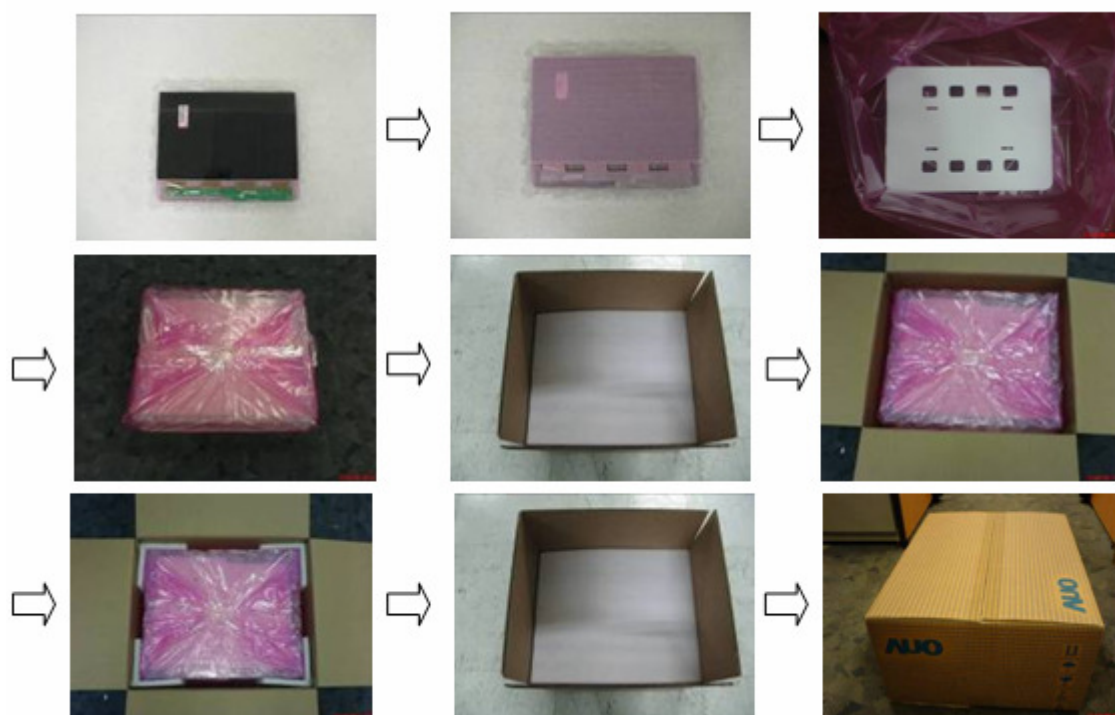




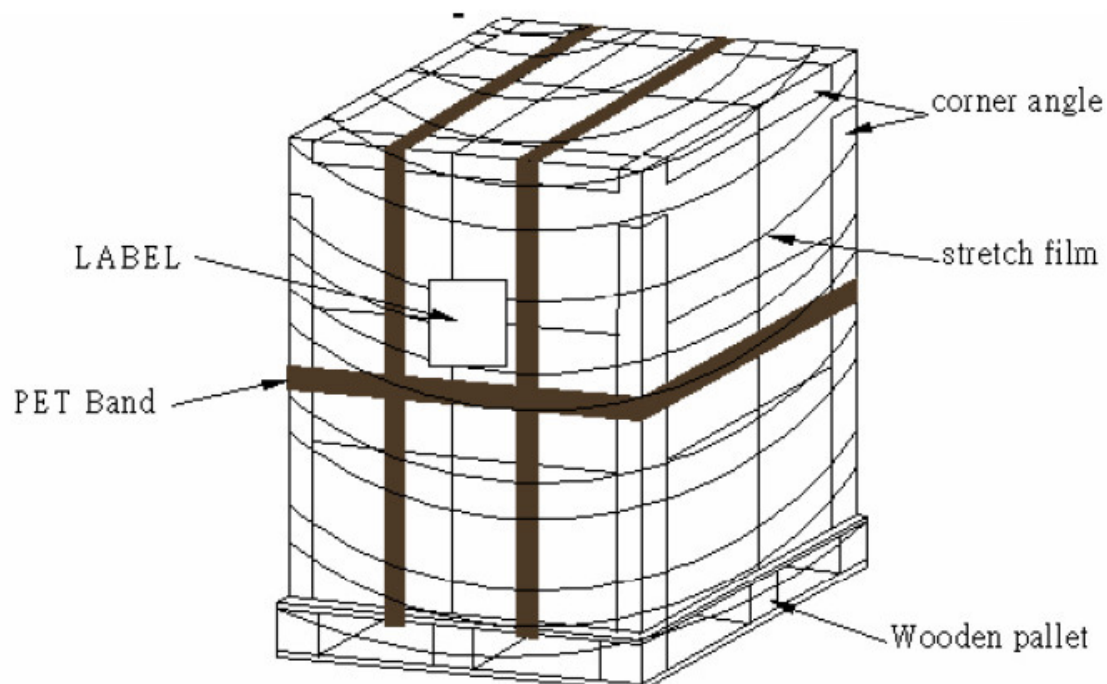
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7.2 Carton Package



7.3 Shipping Package of Palletizing Sequence





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8. Appendix: EDID Description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	2C	00101100	44	
0B	hex, LSB first	42	01000010	66	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	00	00000000	0	
11	Year of manufacture	14	00010100	20	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	03	00000011	3	
14	Video input def. (digital I/P, non-TMDS, CRGB)	80	10000000	128	
15	Max H image size (rounded to cm)	1D	00011101	29	
16	Max V image size (rounded to cm)	10	00010000	16	
17	Display Gamma (=gamma*100)-100	78	01111000	120	
18	Feature support (no DPMS, Active OFF, RGB, tmg Blk#1)	0A	00001010	10	
19	Red/green low bits (Lower 2:2:2:2 bits)	13	00010011	19	
1A	Blue/white low bits (Lower 2:2:2:2 bits)	15	00010101	21	
1B	Red x (Upper 8 bits)	A0	10100000	160	
1C	Red y/ highER 8 bits	58	01011000	88	
1D	Green x	52	01010010	82	
1E	Green y	90	10010000	144	
1F	Blue x	25	00100101	37	
20	Blue y	0F	00001111	15	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	



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26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	12	00010010	18	
37	Pixel Clock/10000 USB	1B	00011011	27	
38	Horz active Lower 8bits	56	01010110	86	
39	Horz blanking Lower 8bits	5A	01011010	90	
3A	HorzAct:HorzBlnk Upper 4:4 bits	50	01010000	80	
3B	Vertical Active Lower 8bits	00	00000000	0	
3C	Vertical Blanking Lower 8bits	19	00011001	25	
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	30	00110000	48	
3E	HorzSync. Offset	30	00110000	48	
3F	HorzSync.Width	20	00100000	32	
40	VertSync.Offset : VertSync.Width	36	00110110	54	
41	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000	0	
42	Horizontal Image Size Lower 8bits	25	00100101	37	
43	Vertical Image Size Lower 8bits	A4	10100100	164	
44	Horizontal & Vertical Image Size (upper 4:4 bits)	10	00010000	16	
45	Horizontal Border (zero for internal LCD)	00	00000000	0	
46	Vertical Border (zero for internal LCD)	00	00000000	0	
47	Signal (non-intr, norm, no stero, sep sync, neg pol)	18	00011000	24	
48	Detailed timing/monitor	00	00000000	0	
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	
4B		0F	00001111	15	
4C		00	00000000	0	
4D		00	00000000	0	
4E		00	00000000	0	
4F		00	00000000	0	
50		00	00000000	0	



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51		00	00000000	0	
52		00	00000000	0	
53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		00	00000000	0	
59		20	00100000	32	
5A	Detailed timing/monitor	00	00000000	0	
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F	Manufacture	41	01000001	65	A
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71	Manufacture P/N	42	01000010	66	B
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	33	00110011	51	3
74	Manufacture P/N	33	00110011	51	3
75	Manufacture P/N	58	01011000	88	X
76	Manufacture P/N	57	01010111	87	W
77	Manufacture P/N	30	00110000	48	0
78	Manufacture P/N	34	00110100	52	4
79	Manufacture P/N	20	00100000	32	
7A	Manufacture P/N	56	01010110	86	V
7B	Manufacture P/N	32	00110010	50	2



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7C		20	00100000	32	
7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	CD	11001101	205	